Application Acceleration within a High-level Language Reconfigurable Computing Framework

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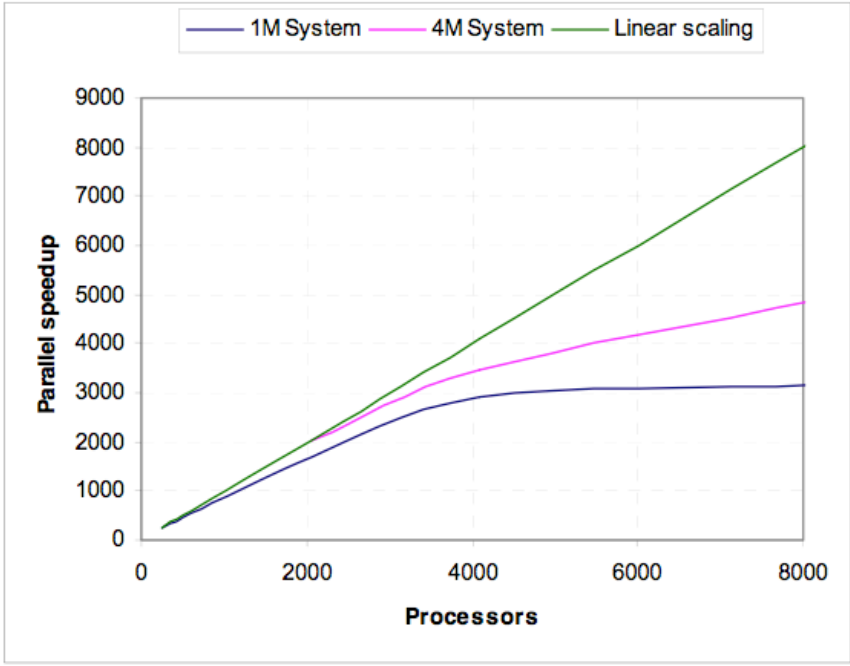
Outline

- Purpose
- Overview of Candidate Application
- Performance Estimation
- Analysis and Conclusion

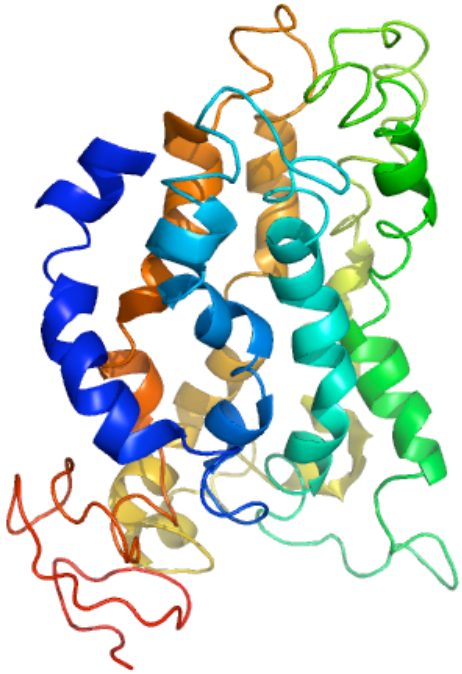
Purpose of Study

- Two challenges to widespread adoption of reconfigurable platforms:
  - Sustained performance in the presence of data transfer overheads
  - Cross-platform HLL SDK
- Why adopt RC platforms?
  - Increase compute power/node
  - Reduce required node-to-node communication



[IBM Corp., 2006]

LAMMPS

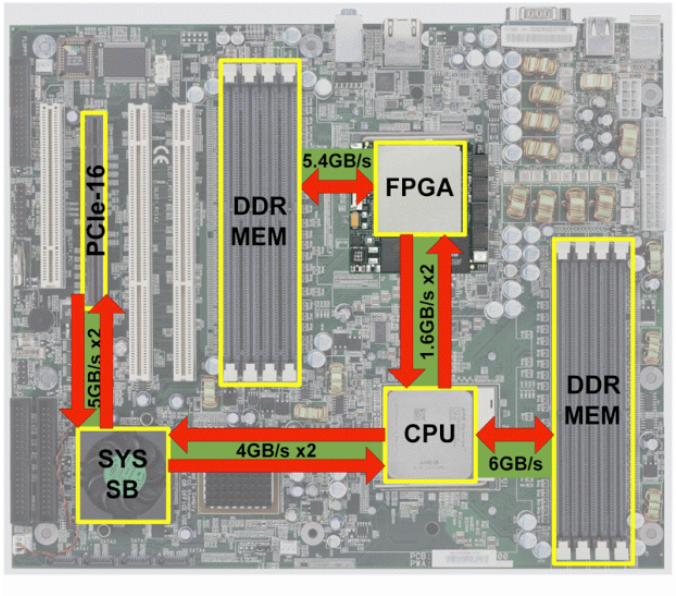


- A molecular dynamics simulator
  - Production application - wanted to examine a *real life* application
  - Used in material science, computational bio, etc.
- Examined LAMMPS for “hot spots” using Xprofiler on a 1.3Ghz IBM Power 4
  - Used Rhodopsin benchmark
- 68% of execution time spent in *pair_lj_charmm_coul_long:compute*
  - Computes the electrostatic and van der Waals forces between ‘pairs’ of atoms
  - The function has 96 double precision multiplies, 7 divides, 81 addition/subtractions

$$E(potential) = \sum_{bonds} f(bond) + \sum_{angles} f(angle) + \sum_{torsions} f(torsion) + \sum_{i=1}^{N}\sum_{j<i}^{N}\left(\frac{A_{ij}}{r_{ij}^{12}} - \frac{B_{ij}}{r_{ij}^{6}}\right) + \sum_{i=1}^{N}\sum_{j<i}^{N}\left(\frac{q_i q_j}{\varepsilon r_{ij}}\right)$$

Target Platform and Tools

- XtremeData XD1000 Development system:
  - Single AMD Opteron™
  - Altera Stratix II FPGA (Opteron socket)
  - HyperTransport™ bus provides 1.6GB/s between FPGA and system hardware
  - 4GB of onboard DDR SDRAM at 5.4GB/s available to FPGA



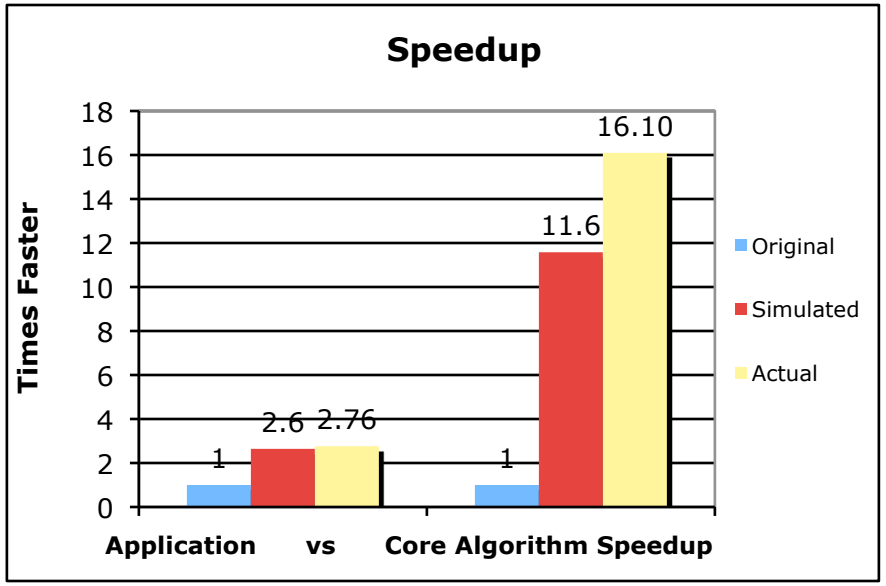
- ImpulseC CoDeveloper Suite
  - Provides C-to-VHDL or Verilog capability
  - Performance estimation of hardware implementation
  - Support for a wide range of target platforms including XtremeData system
  - Reusable modules
  - Single and double precision floating-point support

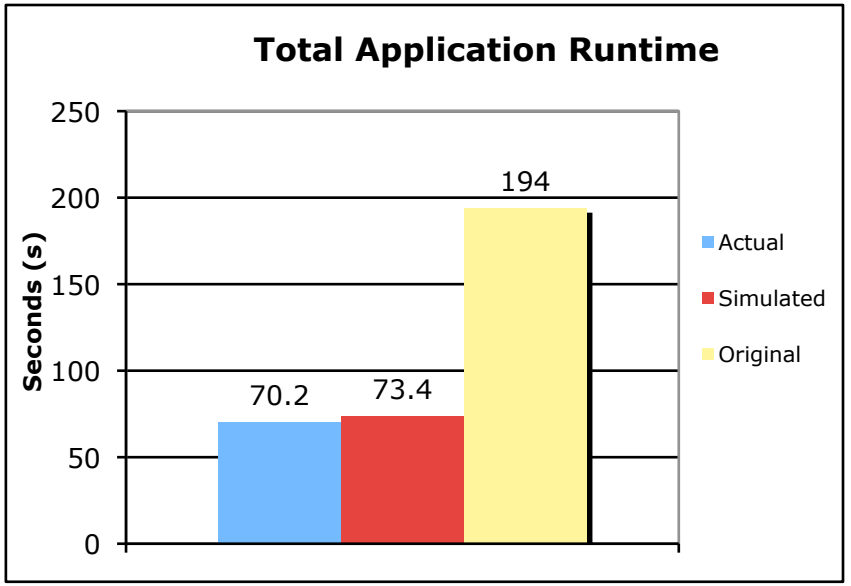
Estimating Performance

- Estimated hardware runtime using StageMaster Explorer:
  - Ported LAMMPS function requires 364 clock cycles to compute forces on one atom
  - FPGA clock rate of 100Mhz → 2.7x speedup for the entire application
    - Clock rate limited by floating point libraries
    - 114ms to compute 1 timestep 32K atoms
      → 11.5x speedup for core algorithm
- Communication bandwidth analysis
  - 5,120,000 double precision floating-point values needed every second → Equates to 40.96 MB/s
  - Theoretical throughput of XtremeData architecture is 800MB/s

Measured Hardware Results

- 164ms mean for 64K atoms (2 timesteps)
- 16x increase for algorithm or 2.77x application speedup*
- Max theoretical obtainable speedup → 3.1x





- * Based on current implementation

Conclusions & Future Work

- Conclusions
  - Almost 3x application speedup
  - Removed computational load from host system and internalized portions of communication
  - Flexible solution, not locked to specific hardware or software
  - Compatible with legacy LAMMPS code
  - No HDL coding - allowing non-HDL-experts to leverage RC platforms for Application Acceleration
- Future Work
  - Streaming and pipelining
  - Performance comparison with similar platforms such as the DRC DS1000

Questions?